#include "p18f452.inc"; include register definition file
 ;PIC18F452 Configuration Bit Settings
 ; Assembly source line config statements
 ; CONFIG1H
 CONFIG OSC = RCIO ; Oscillator Selection bits (RC oscillator w/ OSC2 configured as RA6)
 CONFIG OSCS = OFF ; Oscillator System Clock Switch Enable bit (Oscillator system clock switch
 option is disabled (main oscillator is source))
 ; CONFIG2L
 CONFIG PWRT = OFF ; Power-up Timer Enable bit (PWRT disabled)
 CONFIG BOR = ON ; Brown-out Reset Enable bit (Brown-out Reset enabled)
 CONFIG BORV = 20 ; Brown-out Reset Voltage bits (VBOR set to 2.0V)
 ; CONFIG2H
 CONFIG WDT = OFF ; Watchdog Timer Enable bit (WDT disabled (control is placed on the
 SWDTEN bit))
 CONFIG WDTPS = 128 ; Watchdog Timer Postscale Select bits (1:128)
 ; CONFIG3H
 CONFIG CCP2MUX = ON ; CCP2 Mux bit (CCP2 input/output is multiplexed with RC1)
 ; CONFIG4L
 CONFIG STVR = ON ; Stack Full/Underflow Reset Enable bit (Stack Full/Underflow will cause
 RESET)
 CONFIG LVP = ON ; Low Voltage ICSP Enable bit (Low Voltage ICSP enabled)
 ; CONFIG5L
 CONFIG CP0 = OFF ; Code Protection bit (Block 0 (000200-001FFFh) not code protected)
 CONFIG CP1 = OFF ; Code Protection bit (Block 1 (002000-003FFFh) not code protected)
 CONFIG CP2 = OFF ; Code Protection bit (Block 2 (004000-005FFFh) not code protected)
 CONFIG CP3 = OFF ; Code Protection bit (Block 3 (006000-007FFFh) not code protected)
 ; CONFIG5H
 CONFIG CPB = OFF ; Boot Block Code Protection bit (Boot Block (000000-0001FFh) not code
 protected)
 CONFIG CPD = OFF ; Data EEPROM Code Protection bit (Data EEPROM not code protected)
 ; CONFIG6L
 CONFIG WRT0 = OFF ; Write Protection bit (Block 0 (000200-001FFFh) not write protected)
 CONFIG WRT1 = OFF ; Write Protection bit (Block 1 (002000-003FFFh) not write protected)
 CONFIG WRT2 = OFF ; Write Protection bit (Block 2 (004000-005FFFh) not write protected)
 CONFIG WRT3 = OFF ; Write Protection bit (Block 3 (006000-007FFFh) not write protected)
 ; CONFIG6H
 CONFIG WRTC = OFF ; Configuration Register Write Protection bit (Configuration registers
 (300000-3000FFh) not write protected)
 CONFIG WRTB = OFF ; Boot Block Write Protection bit (Boot Block (000000-0001FFh) not write
 protected)
 CONFIG WRTD = OFF ; Data EEPROM Write Protection bit (Data EEPROM not write protected)
 ; CONFIG7L
CONFIG EBTR0 = OFF ; Table Read Protection bit (Block 0 (000200-001FFFh) not protected from Table Reads executed in other blocks)
CONFIG EBTR1 = OFF ; Table Read Protection bit (Block 1 (002000-003FFFh) not protected from Table Reads executed in other blocks)
CONFIG EBTR2 = OFF ; Table Read Protection bit (Block 2 (004000-005FFFh) not protected from Table Reads executed in other blocks)
CONFIG EBTR3 = OFF ; Table Read Protection bit (Block 3 (006000-007FFFh) not protected from Table Reads executed in other blocks)

; CONFIG7H
CONFIG EBTRB = OFF ; Boot Block Table Read Protection bit (Boot Block (000000-0001FFh) not protected from Table Reads executed in other blocks)

; VARIABLES
  RS EQU 5
  RW EQU 6
  EN EQU 7
  ORG 0x0
  CLRF TRISC
  CLRF TRISD
  MOV LW 0X38
  CALL LCD_COMMAND
  MOV LW 0X38
  CALL LCD_COMMAND
  MOV LW 0X38
  CALL LCD_COMMAND
  MOV LW 0X6
  CALL LCD_COMMAND
  MOV LW 0X0C
  CALL LCD_COMMAND
  MOV LW 0X01
  CALL LCD_COMMAND
  MOV LW 0X0F
  CALL LCD_COMMAND
  CALL DELAY
  MOV LW 'G'
  CALL LCD_DATA
  CALL DELAY
  MOV LW 'A'
  CALL LCD_DATA
  CALL DELAY
  MOV LW 'U'
  CALL LCD_DATA
  CALL DELAY
  MOV LW 'N'
  CALL LCD_DATA
  CALL DELAY
MOVLW Oxc0
CALL LCD_COMMAND
CALL DELAY
; second line
MOVLW 'E'
CALL LCD_DATA
MOVLW 'E'
CALL LCD_DATA
MOVLW '.'
CALL LCD_DATA
MOVLW ' ' 
CALL LCD_DATA
MOVLW 'E'
CALL LCD_DATA
MOVLW 'N'
CALL LCD_DATA
MOVLW 'G'
CALL LCD_DATA
MOVLW '.'
AGAIN BTG PORTC,RS
   BRA AGAIN ; TO STAY HERE

; COMMAND SUBROUTINE
LCD_COMMAND
MOVWF PORTD
BCF PORTC,RS
CALL DELAY
BCF PORTC,RW
CALL DELAY
BSF PORTC,EN
CALL DELAY
BCF PORTC,EN
CALL DELAY
RETURN

; DATA SUBROUTINE
LCD_DATA
MOVWF PORTD
BSF PORTC,RS
CALL DELAY
BCF PORTC,RW
CALL DELAY
BSF PORTC,EN
CALL DELAY
BCF PORTC,EN
CALL DELAY
RETURN
;DELAY SUBROUTINE
DELAY
MOV LW 0X40
MOVWF 0X50
XX DECFSZ 0X50,F
BRA XX
RETURN
END